WHAT IS CLAIMED IS:

1. An apparatus for passing interrupts from one or more devices configured for a specific interrupt architecture to one or more processors not designed for the specific interrupt architecture, comprising:

an abstraction layer comprising a first plurality of registers conforming to the specific interrupt architecture; and

an implementation dependent layer, disposed in communication between the abstraction layer and the one or more processors, comprising a second plurality of registers which correspond to the first plurality of registers, wherein the implementation dependent layer is configured to receive interrupts and forward received interrupts to the one or more processors and to read and write data to the second plurality of registers in response to interrupts processed through the one or more processors.

2. The apparatus of claim 1, further comprising a register access generator connected to provide data and control signals to the implementation dependent layer and to provide address accesses to the abstraction layer.

3. The apparatus of claim 2, further comprising a processor bus interface connected to provide communication between the register access generator and the one or more processors.

4. The apparatus of claim 3, wherein the implementation dependent hardware layer further comprises an arbitration logic circuit for determining a source of an interrupt and a targeted processor.

5. The apparatus of claim 4, wherein the arbitration logic circuit is connected to an on-board interrupt generation logic circuit, an input/output interrupt generation logic circuit and an inter-processor interrupt generation logic circuit.

6. The apparatus of claim 5, wherein the implementation dependent hardware layer further comprises a register control logic circuit for controlling data read and write functions to the second plurality of registers, the register control logic circuit configured to receive control signals from the register access generator and address decodes from one or more address decoders in the abstraction layer.

7. The apparatus of claim 6, wherein the implementation dependent hardware layer further comprises one or more presentation logic circuit connected respectively to external interrupt inputs of the one or more processors.

8. The apparatus of claim 1, wherein the specific interrupt architecture is an Advanced Programmable Interrupt Controller (APIC) architecture.

9. The apparatus of claim 8, wherein the first plurality of registers comprises one or more register sets in full compliance with the APIC architecture.

10. The apparatus of claim 8, wherein the first plurality of registers comprises one or more register sets which provide operational similarity with the APIC architecture.

11. The apparatus of claim 8, wherein the one or more processors are PowerPC processors.

12. A method for passing interrupts from one or more devices configured for a specific interrupt architecture to one or more processors not designed for the specific interrupt architecture, comprising:

providing an abstraction layer comprising a first plurality of registers conforming to the specific interrupt architecture;

providing an implementation dependent layer, disposed in communication between the abstraction layer and the one or more processors, comprising a second plurality of registers which correspond to the first plurality of registers;

receiving interrupts and forwarding received interrupts to the one or more processors through the implementation dependent layer; and

reading and writing data to the second plurality of registers in response to interrupts processed through the one or more processor.

13. The method of claim 12, further comprising providing a register access generator connected to provide data and control signals to the implementation dependent layer and to provide address accesses to the abstraction layer.

14. The method of claim 12, wherein the specific interrupt architecture is an Advanced Programmable Interrupt Controller (APIC) architecture and the one or more processors are PowerPC processors.

15. An apparatus for passing interrupts from one or more devices configured for a specific interrupt architecture to one or more processors not designed for the specific interrupt architecture, comprising:

an abstraction layer comprising a plurality of address decoders and a first plurality of registers conforming to the specific interrupt architecture;

an implementation dependent layer, disposed in communication between the abstraction layer and the one or more processors, comprising a second plurality of registers which correspond to the first plurality of registers, wherein the implementation dependent layer is configured to receive interrupts and forward received interrupts to the one or more processors and to read and write data to the second plurality of registers in response to interrupts processed through the one or more processor; and

a register access generator, disposed in communication with the one or more processors, configured to provide data and control signals to the implementation dependent layer and to provide address accesses to the abstraction layer.

16. The apparatus of claim 14, further comprising a processor bus interface to provide communication between the register access generator and the one or more processors.

17. The apparatus of claim 14, wherein the implementation dependent hardware layer further comprises:

an arbitration logic circuit for determining a source of an interrupt and a targeted processor;

a register control logic circuit for controlling data read and write functions to the second plurality of registers, the register control logic circuit configured to receive control signals from the register access generator and address decodes from one or more address decoders in the abstraction layer; and

one or more presentation logic circuit connected respectively to external interrupt inputs of the one or more processors.

18. The apparatus of claim 17, wherein the arbitration logic circuit is connected to an on-board interrupt generation logic circuit, an input/output interrupt generation logic circuit and an inter-processor interrupt generation logic circuit.

19. The apparatus of claim 14, wherein the specific interrupt architecture is an Advanced Programmable Interrupt Controller (APIC) architecture and the one or more processors are PowerPC processors.

20. The apparatus of claim 19, wherein the first plurality of registers comprises one or more register sets in full compliance with the APIC architecture.

21. The apparatus of claim 19, wherein the first plurality of registers comprises one or more register sets which provide operational similarity with the APIC architecture.